LG480

Pattern Generator
Logic Analyzer

ADM

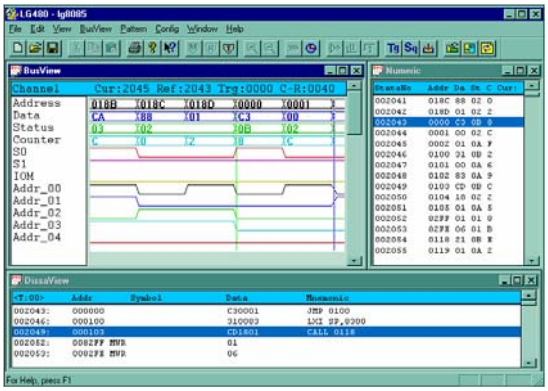
Innovative Powerful & User friendly Embedded Development Tool

Features for Hardware & Software Designer

LG480 Embedded Debug Tools operates under Microsoft Windows™ and offer a wide combination of Logic Analyzer and Pattern Generator configuration's which are easy to use and provide many features for the hardware and software designer of embedded systems.

The LG480– 48 I/O channels can simultaneously output test vectors and capture the digital response in real time. Special Disassembly pods are available for 8 and 16 bit Processors and Controllers. SOC adapter is available to probe FPGA/ASCII chips.

Record data from your system in real time and analyze this data by using your symbolic addresses and High Level Language Source Code.



100Mhz & 128K Memory

For general purpose logic analysis, configure LG480 to 25Mhz on all 48 channels or 100Mhz for high speed critical applications

If debugging of your application requires very large memory, LG480 offers you 128K memory as standard. But don't waste time for waiting until these large amount of data is displayed if you don't need it. Just reduce the memory depth with a mouse click and save time.

Easy to Use Interface

LG480 operates under Microsoft Windows™ 95/98 or Windows NT/XP.

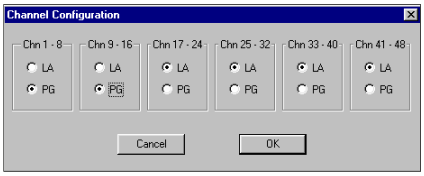
All data and setup displays offer an intuitive setting of parameters and powerful data analysis.

Each data display allows multiple display of either the same data or different data sets.

Cursors can be linked to point to the same data in different views. Context sensitive help provides fast online information.

Configure the System to meet Your Needs

To meet the needs of your design, configure LG480 as 48 channel Logic Analyzer, or as 48 channels of Pattern Generator, or a combination of Logic Analyzer & Pattern Generator.



Easy Documentation

Documentation is as easy as the push of a button! Just copy the screen contents into the Clipboard and paste it into your favorite word processor.

In addition, the Timing View offers a Preview option. Any Windows compatible printer is supported.

48 Channels of Logic Analysis

The LG480 features 48 channels of Logic analysis with disassembly support for most popular 8 and 16 bit processor with 128K deep trace buffer.

All debugging and trace information can be displayed at assembler level, numeric, waveform or as High level language. A unique single probe connection allows the user to collect data in State or Timing mode.

48 Channels of Pattern Generation

The LG480 Pattern generator provides 48 fully programmable data stimulus for active testing of your system.

Pattern data can be easily generated by either directly importing Logic Analyzer traces or by using a variety of built in Pattern generation menu options.

Simulator Outputs in ASCII format may also be imported .

SOC Adaptor

The SOC adaption is a simple way of analyzing internal nodes in FPGAs or ASICS.

By integration of a Logic Analyzer, Pattern Generator and a scanner module, up to 1024 channels can be traced inside a silicon system.

The SOC adaption is scalable up to 32 multiplexed signals.

Symbolic Debugging

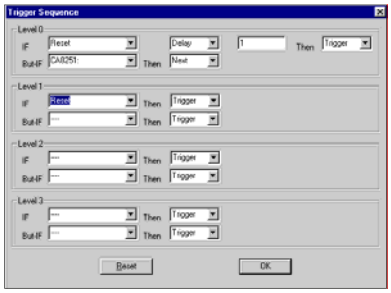
A variety of Symbol converters is available including a standard LG480 format. The number of Symbols is unlimited. The Trigger Word Dialog Box includes a Symbol Browser for comfortable Symbolic Triggering.

Converter for Xilinx is also included to facilitate mapping and selection of physical channels.

Trigger on a Source Code Line

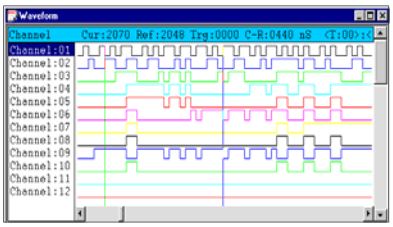
To make debugging even more comfortable, the HLL-Manager has a built in Trigger Window. This Trigger Window allows setting Trigger points to a specific Source Code Line. No more manual Trigger SetUps are required. After loading a suitable Setup the Triggerword is set directly to the Source Code Line and a recording is started.

Powerful Trigger Sequence



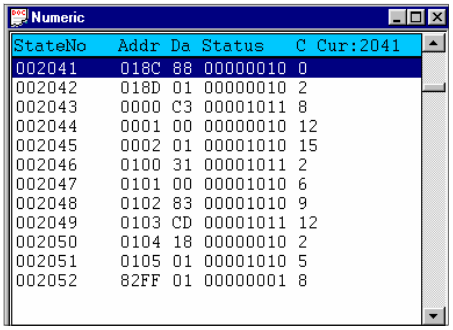
The sequence dialog box defines the sequence of occurrence of the trigger events defined in the Trigger Dialog box. Up to 4 levels of Trigger sequence can be programmed in an easy to understand **If…then… ButIf...** Format. A 64K event counter/ delay is also available for the first level of Trigger sequence.

Waveform View



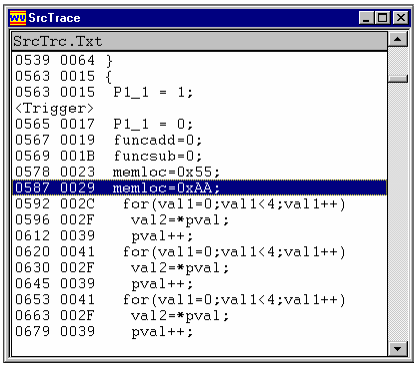
This screen shows upt to 32 channels and lets you assign names to physical channel, rename signals and group signals into busses. The window also lets you zoom in on a area of interest. Markers and Cursors are provided to show the value at the specified time location.

Numeric View



In this view, the channels are grouped and displayed as numeric values, namely hex, decimal, octal and binary.

High Level Language Debugging

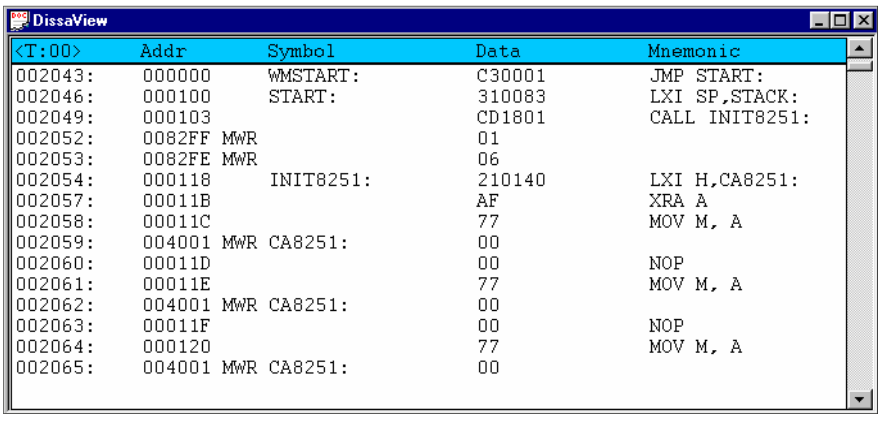


The High Level Language Manager correlates recorded processor data to High Level Source Code.

The HLL-Manager is an independent Windows program and communicates with the Logic Analyzer using the Software Interface of the system. Setting the Cursor to a recorded processor address in one of the data views like Timing, List or Disassembler causes the HLL-Manager to display the corresponding Source Code Line.

The HLLManager is designed very flexibly, so that it can be easily adapted to the various Compilers and Processors during run time.

Powerful Disassemblers



LG480 Disassemblers support most of today's 8/16 bit Embedded Control- and High Performance Micro Processor families.

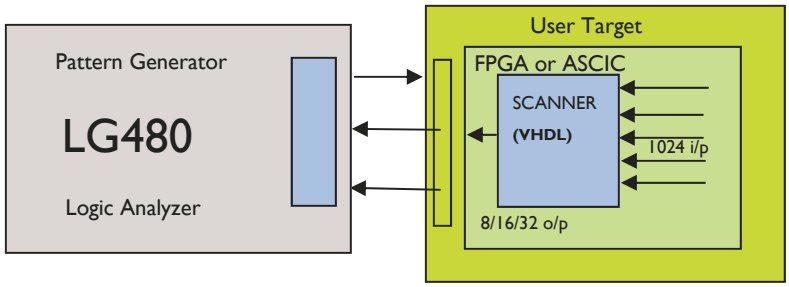
All Disassemblers are developed to meet the requirements of the "Flexible Adaption Concept" and to generate as much information as possible. Pipelined processor activity and non-executed instructions as well as jumps are detected and marked in the disassembler listing. The Disassembly Pod can also be effectively used to capture real time timing waveforms.

Pattern Generator

As the complexity of digital circuits increases continuously, the cost of device testing has also increased sharply. The increasing complexity of testing has shifted more and more of the testing responsibility towards the design engineers.

LG480 with built in Pattern Generator and Logic Analyzer forms a *virtual ATE* system. The user prototype system accepts simulation output and generates commands to configure the Pattern Generator and Logic Analyzer. The DUT (Device Under Test) receives stimulus from the patter generator and generates output response to the Logic Analyzer. The actual response captured by the Logic Analyzer can be fed into simulation software for further processing. The simulation system can display a graphical comparison of the expected output waveforms (from the simulation) and the actual response waveforms from logic analyzer.

SOC Adapter



The adpater for SOC Trace enables trace of internal signals in FPGA and ASIC devices. The trace data are sampled inside the chip and send-out on up to 32 multiplexed analyzer channels. The multiplexer is controlled by LG480. If all channels are inside one 32 bit block, the logic analysis can run at full speed. If signals out of two groups should be sampled at the same time, the sample rate is halved. Up to 1024 channels can be traced by the scanner module. The scanner module has up to 1024 signal inputs for customer usage, 2 control lines for programming, one clock input for the scanner clock, one reference clock output, a synchronization signal and up to 32 multiplexed trace signals. The scanner module code can be written in VHDL or ABEL.

Features:

- 48 Channels x 128K Logic Analyzer.
- 48 Channels x 128K Pattern Generator.
- Pattern Waveform Editor.
- Ready to use Standard Patterns like Counters,Clocks etc.
- Supports Xilinx WebPack Software.
- Multiple display cursor with real time readout.
- Color Coded signals and probes.
- Multiple Reference buffer 48 x 128K.
- Display State Data in Hex, Binary, Octal , Decimal .
- Sixteen 48 bit Trigger Word with 65535 delay/event counter.
- 4 Level Trigger with IF-THEN-BUTIF sequencing.
- 16 Trigger Delay modes.
- Export Data to popular Spreadsheets & Wordprocessor.
- 8 bit Disassembler support for 8085,Z80,6502,6809,MCS51.
- 16 bit Disassembler support for 8088,8086,68000,68010.
- SOC Adaptor support.
- CPLD Trainer Board with JTAG Programmer and cables.

LG480	Logic Analyzer	Pattern Generator
Channels	48	48
Memory	128K	128K
Speed	upto 100Mhz	upto 50Mhz
Trigger Sequence	4 level IF-THEN-BUTIF	N.A
Event/Delay Counter	65535	N.A
Disassembler	8/16 bit	N.A

About ADM™

Over a decade ADM (Applied Digital Microsystems Pvt Ltd.) has been manufacturing a range of high performance debugging tools such as Cross Compilers, Emulators (8085 upto Pentium) , Logic Analyzers/Pattern Generator (Upto 1Ghz - 512 channels /2MB), Graphic Tablets (upto A0 Size) and hand held Digital Storage Oscilloscopes (Upto 100Mhz) and is dedicated to provide quality product & support.

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